electric resistances R34 and R36. Therefore, even if the electric resistance R32 changes due to the piezoresistance effect, an amount of change in the forward voltage drop V_F is extremely small.

Since the amounts of change in the electric resistances R32, R34, R36, and R38 due to the piezoresistance effect are thus small, the forward voltage drop V_F hardly changes due to the piezoresistance effect. Therefore, in the semiconductor device **10**, even application of stress to the diode **30** hardly causes a deviation in the correlation between the forward voltage drop V_F and the temperature. Therefore, use of the diode **30** makes it possible to control the IGBT **62** accurately depending on the temperature of the semiconductor substrate **12**.

Next, a method for manufacturing the semiconductor device **10** is described. First, the insulating layer **20** is formed on a portion of the semiconductor substrate **12**. Next, the cathode electrode **32** and the gate wires **22** are formed on the insulating layer **20**. The cathode electrode **32** and the gate wires **22** are both formed with n-type polysilicon. The cathode electrode **32** and the gate wires **22** can be simultaneously formed by CVD. Next, the n-type semiconductor layer **34** (which is an n-type polysilicon layer) and the p-type semiconductor layer **36** (which is a p-type polysilicon layer) are formed in sequence by CVD. It should be noted that the n-type semiconductor layer **34** and the p-type semiconductor layer **36** may each be formed by implanting n-type or p-type impurities into a polysilicon layer formed by CVD. Next, the structure on an upper surface **12***a*side of the IGBT **62** (i.e. the emitter region, the body region, the trenches, the gate insulating films, and the gate electrodes) is formed in the semiconductor substrate **12**. It should be noted that the gate electrodes are formed by polysilicon. Further, the emitter region and the body region are formed by implanting ions into the semiconductor substrate **12**. In activating the ions implanted in the semiconductor substrate **12**, the semiconductor substrate **12** is heat-treated. At this occasion, if a metal layer is formed on the surface of the semiconductor substrate **12**, the metal may diffuse into the semiconductor substrate **12** and thus may make it impossible to control the characteristics of the semiconductor substrate **12** as intended. Further, a furnace for use in heat treatment may be contaminated by the metal. Contrary to this, in this manufacturing method, no metal layer is present on the surface of the semiconductor substrate **12** at the time of heat treatment, as the cathode electrode **32** is configured of n-type polysilicon. This makes it possible to prevent metal from diffusing into the semiconductor substrate **12** and prevent the furnace from being contaminated by metal. Once the structure on the upper surface **12***a*side of the IGBT **62** is completed, the emitter electrodes **16***a*and **16***b*, the anode electrode **38**, and the cathode wiring layer **40** are formed with metal. Next, the insulating layer **24** is formed. Next, the structure on a lower surface **12***b*side of the IGBT **62** (i.e. the collector region, the collector electrode **18**, etc.) is formed. Thereafter, for example by connecting the heatsink **50** to the emitter electrodes **16***a*and **16***b*, the semiconductor device **10** is completed.

As described above, the cathode electrode **32**, which is the layer in the stacked structure of the diode **30** that is closest to the semiconductor substrate **12**, is configured of an n-type polysilicon layer. For this reason, even if heat treatment is performed after the formation of the cathode electrode **32**, the semiconductor substrate **12** and the furnace are not contaminated by metal. Therefore, by forming the metal electrodes (i.e. the emitter electrodes **16***a*and **16***b*, the anode electrode **38**, etc.) after the heat treatment, contamination of the semiconductor substrate **12** and the furnace by metal can be prevented. Further, since carriers in the cathode electrode **32** (which is an n-type polysilicon layer) are electrons, the electric resistivity (i.e. the electric resistance R32) of the cathode electrode **32** can be easily lowered. Therefore, the amount of change in the electric resistance R32 of the cathode electrode **32** due to the piezoresistance effect can be made smaller, and accordingly a change in the forward voltage drop V_F due to the piezoresistance effect can be suppressed. It should be noted that in a case where metal contamination is not a problem, the cathode electrode **32** may be configured of metal.

In a semiconductor device **10** according to a modification, the layers of the diode **30** may be stacked in an order opposite to the order in which they are stacked in the aforementioned embodiment. That is, beginning from the semiconductor substrate **12** side, the anode electrode **38**, the p-type semiconductor layer **36**, the n-type semiconductor layer **34**, and the cathode electrode **32** may be stacked in this order. Even such a configuration can better suppress the influence of the piezoresistance effect than the conventional diode. In this case, however, it is necessary to provide the anode electrode **38** with an extension portion by making the anode electrode **38** wider than the other layers. This causes the reference current I_F to flow through the extension portion of the anode electrode **38** in the planar direction. Further, in this configuration, it is preferable that the anode electrode **38** is formed by polysilicon having a high density of p-type impurities in order to prevent the metal contamination at the time of heat treatment in the manufacturing process. In this case, the electric resistance of the anode electrode **38** is higher than the electric resistance R32 of the cathode electrode **32** in the aforementioned embodiment, as carriers in the p-type polysilicon are holes. For this reason, in the semiconductor device according to the modification, the anode electrode **38** is influenced by the piezoresistance effect, and the forward voltage drop V_F more easily changes due to the piezoresistance effect than in the aforementioned embodiment. Therefore, the aforementioned embodiment can more effectively suppress the influence of the piezoresistance effect than the semiconductor device according to the modification.

In the aforementioned embodiment, the IGBTs are formed in the semiconductor substrate **12**. Alternatively, the IGBTs may be replaced by other switching elements (e.g. MOSFETs) formed in the semiconductor substrate **12**. Alternatively, the IGBTs may be replaced by elements other than switching elements formed in the semiconductor substrate **12**.

Some of the following enumerates technical elements disclosed herein. It should be noted that the following technical elements are each independently useful.

A semiconductor device disclosed in the present disclosure as an example may further comprise a heatsink connected to the semiconductor substrate at positions located on both sides of the temperature sense diode.

When the heatsink is connected to the semiconductor substrate in this manner, the difference in amount of thermal expansion between the heatsink and the semiconductor substrate causes higher stress to be applied to the temperature sense diode. In such a structure in which stress is easily applied to the temperature sense diode, the influence of the piezoresistance effect can be more effectively suppressed by employing a stacked structure in which the anode electrode, the p-type semiconductor layer, the n-type semiconductor layer, and the cathode electrode are stacked along the thickness direction of the semiconductor substrate.